ESD Phenomena in Interconnect Structures

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Abstract – Interconnect forms a part of all ESD protection networks. ESD discharges can cause both latent and permanent damages in interconnect structures. ESD discharges, that barely affect the resistance of a structure, can reduce the electromigration lifetime of metal structures by more than a factor 100. Also snapback behavior, which limits the ESD robustness of silicon based interconnect structures, is observed. With this knowledge designs can be optimized for area and robustness.

I. Introduction

Interconnect inherently forms part of any ESD protection network. Especially the backend metallization has received much attention in the recent past [1]-[9]. Typically the design target within a dedicated ESD protection is that interconnect will not be the limiting factor for the robustness, although it has been argued that it will become dominant in modern technologies [6]. Thus it is important to know and understand the ESD phenomena in interconnects to determine design rules in the ESD protection area. This allows the designer to optimize area and electrical performance. Also a good understanding of the properties will help problem analysis within products.

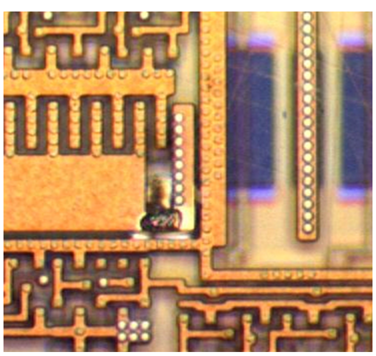

Figure 1: Circuit fail after ESD qualification. Damage was found in a metal 1 interconnect.

Usually a metal fail has the form of an open connection, as illustrated in Figure 1. ESD stress on metal interconnect has also been reported to lead to changes in the line resistance [1]-[9], increased noise [8] and reduced electromigration lifetime [1], [3], [9]. Detailed analytical models [1], [2] and pragmatic approximations [3] have been proposed to describe the behavior.

Much less attention has been attributed to the behavior of silicided and unsilicided silicon interconnects [10], although the impact of silicidation on ESD behavior of active devices has been studied extensively [11], [12]. This kind of lines will typically be used for local interconnections only.

This paper presents concise results on metal (Al and Cu), polysilicon, silicided and unsilicided diffusion lines. It will be shown that, besides direct hard ESD damage, also latent damage is observed. It is also shown that successive stresses lead to cumulative damage. It will be shown that this damage has a larger impact on the electromigration reliability of the structures than reported before. The correlation between Human Body Model (HBM) and Transmission Line Pulse Testing (TLP) will be established for these structures. Using the data obtained, robust designs can be realized with greater success rate.

II. ESD Characterization

All TLP data is taken with 100 ns wide, 10 ns rise time pulses using a 500 Ω system. Normally, after each TLP pulse a leakage current is measured to evaluate device damage. In this case after each TLP pulse, the low current DC resistance of the structure is measured, after sufficient delay to cool down the structure. Thus this measurement shows permanent changes in the resistance of the structure. In this study straight interconnect lines of different W and L are

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used. Typically with W scaling the W/L ratio is kept constant with an extra structure to study the L effect. Important distinctions can be made between the behavior of metal based and silicon based interconnect.

A. Metal based interconnect

The TLP characteristics for all metal structures are very similar. A typical example is given in Figure 2. The I-V curves are constructed using data taken at the start and end of the pulse. The effect of heating is clearly visible by the difference in the 2 curves at medium and high current levels. The development of the low current DC resistance as a function of the TLP stress is also presented. Clearly the transition from 'undamaged' to 'open connection' happens quite suddenly at a given current. There are permanent changes in resistance before that moment, but they are so small that they will not lead to a functional failure in circuits. The slope of the TLP curves at low current levels agrees with the DC measured resistance value.

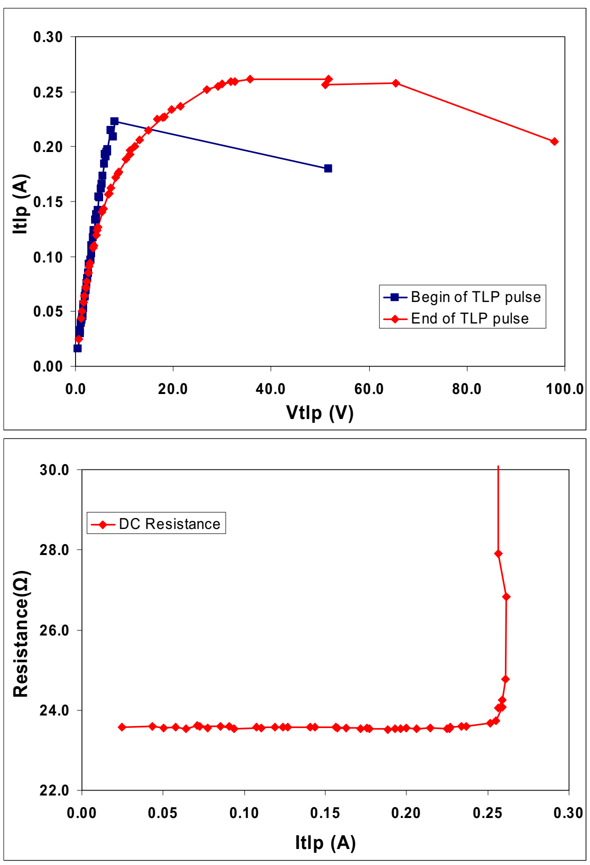

Figure 2: Typical example of TLP characteristics for metal interconnect, I-V curves (top) and DC resistance development (bottom).

After TLP stress two distinct types of damage have been observed optically: discolorized spots and open connections (see also Figure 16). It has been observed that the discolorization is already present before the fatal damage occurs. In some cases the open developed at a discolorized spot that was formed at lower stress levels.

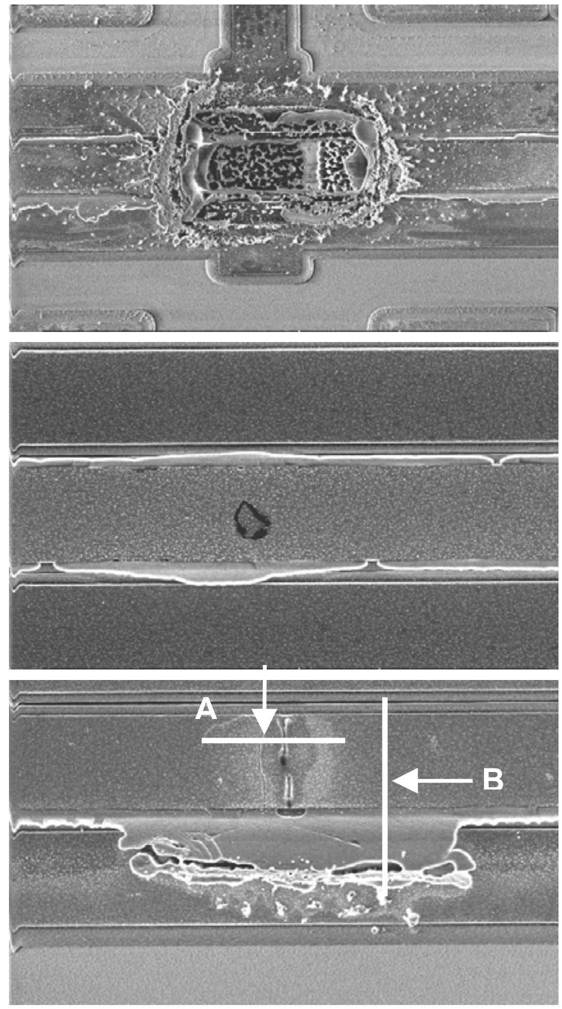

Figure 3: 3 different failures in 3 µm Al line after TLP stress. This sample received 6 high current pulses before it failed. A and B indicate positions of cross-sections shown in Figure 4.

Figure 3 shows SEM pictures of an Al line, taken after removing all layers on top of the metal by plasma etching. This sample was subjected to 6 consecutive TLP pulses very close to the failure level. After 6 pulses it developed an open connection. After inspection 6 damaged sites were found. Some would relate to an open connection, some would not.

Metal extrusions are observed in many locations along the metal line especially where clear defects in metal are visible. FIB cross-sections and top views are made to characterize those observed damaged sites. It is found that those damages, even if they look small, correspond with large voids in the metal, as shown in Figure 4. This suggests that the metal line must have been melted during the stress which leads to the formation of metal extrusions and consequently voids in the metal line. Those voids are expected to reduce the EM lifetime.

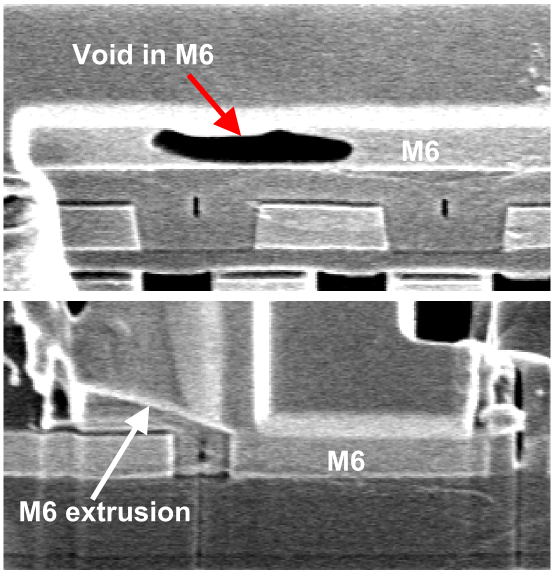

Figure 4: FIB cross section on position A (top) and B (bottom) indicated in Figure 3.

B. Silicon based interconnect

In this section the results obtained on silicon based interconnect (unsilicided polysilicon, unsilicided diffusion and silicided diffusion lines) are discussed. All structures were N-type doped. The TLP characteristics of these structures are similar to each other, but significantly different from those of metal structures. An example is given in Figure 5 for an unsilicided N-type polysilicon structure. The most striking difference with the metal-based structures is the 'snapback-like' behavior, which has been found for all silicon based structures. The characteristics are similar to those observed in [10] for silicided interconnects. Interestingly we see the same behavior for **UN**silicided structures.

As for the metal structures, permanent changes in the low current resistance are found. However the resistance development is more gradual and occasionally starts with a small decrease, before it increases and becomes an open connection. The snapback leads to the first permanent change in the resistance. This can be considered as a soft fail. However, the fatal current, Ifail, lies at a much higher level. Although the changes before destruction are much larger than for metal lines, in many designs they will not immediately lead to functional failures.

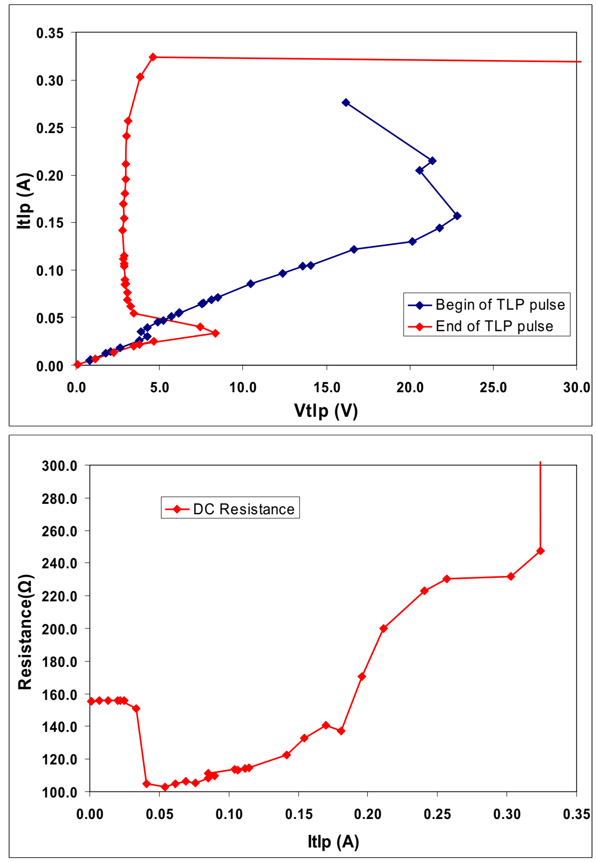

Figure 5: Typical example of TLP characteristics for silicon based interconnect, I-V curves (top) and DC resistance development (bottom).

The snapback is a repeatable phenomenon. Figure 6 shows I-V curves taken successively on a single sample. Clearly the snapback phenomenon is intrinsic to the structure and does not disappear due to the damages leading to the resistance change. Figure 7 presents the normalized I-V characteristics for several unsilicided polysilicon structures. The snapback happens at a constant current density. The voltage at snapback scales linearly with the length of the structure. This suggests a heat driven mechanism or an avalanche mechanism within the structure [14]. After this mechanism localized heating finally causes a fatal failure.

Figure 5 to Figure 7 are all obained on polysilicon structures. For diffusion type interconnects the same behavior is found. Figure 8 compares the normalized curves for unsilicided polysilicon, unsilicided diffusion and silicided diffusion structures. It is clear that the silicided and unsilicided diffusion structures show a snapback at a different current density.

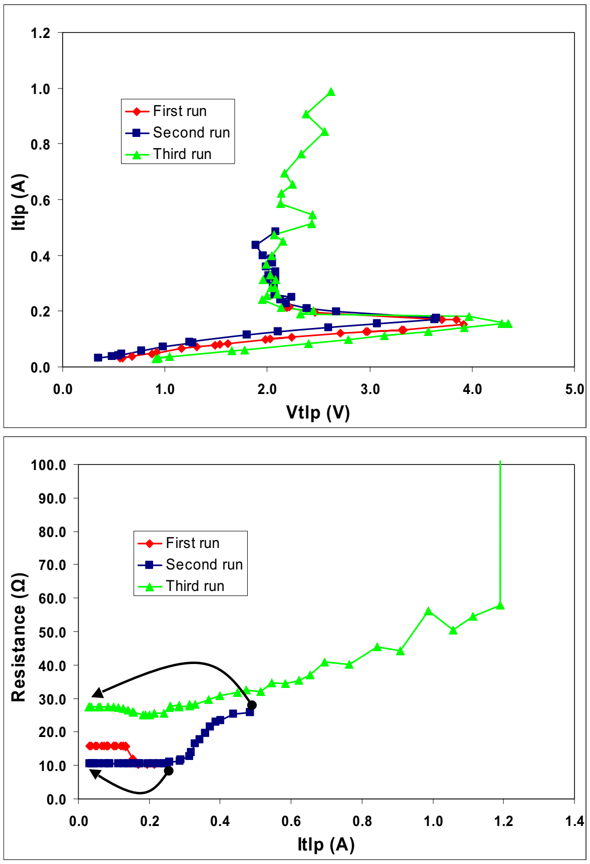

Figure 6: TLP characteristics of successive measurements on the same sample.

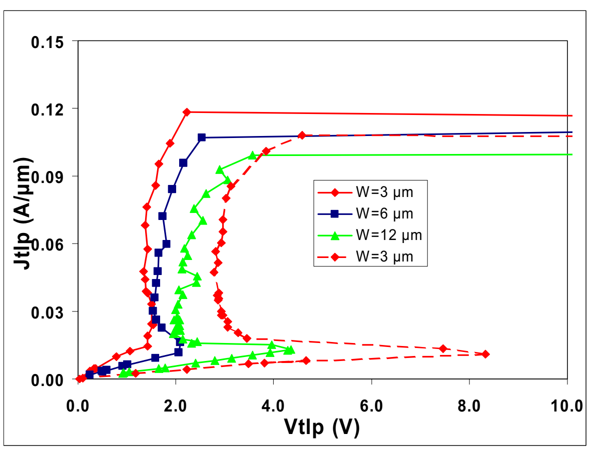

Figure 7: Normalized I-V TLP characteristics for polysilicon structures of different widths. The dashed line indicates a structure with 10 times higher resistance than the other 3 structures.

At room-temperature the ratio between the sheet resistances is approximately 1:10. Therefore about 10% of the current will flow through the diffusion part in the case of a silicided structure. Due to self-heating the temperature will rise considerably. Since the temperature coefficient of the resistivity of silicide is approximately 3 times larger than that of silicon, gradually a larger part of the current will flow through the silicon. Thus the ratio of the snapback current densities will be much smaller than that of the sheet resistances at room temperature.

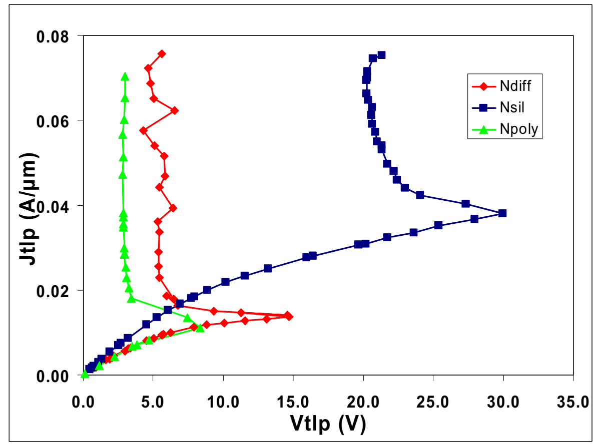

Figure 8: Normalized I-V TLP characteristics for 3 different silicon based structures.

In [10] it is argued that the snapback in the diffusion structures is related to junction breakdown between the N-diffusion and the substrate. This is not the case in our structures. As is shown in Figure 8 voltages that are much higher than the junction breakdown voltage (about 5 V in this technology) are observed. Also the same mechanism is found in polysilicon structures. Since these are placed on field oxide, they are completely isolated from the substrate. Junction breakdown is not possible here. In addition, lateral damage (filaments in the direction of the current flow through the resistor) has been observed for those structures. This does not agree with a vertical breakdown of the junction. SEM pictures of TLP stressed samples (both silicided and unsilicided) are given in Figure 9. These are taken after the oxide has been removed with HF and additional contrast etch to make damages more visible. All photographs are from samples that were not stressed until a complete open failure.

C. Scaling

Taking the (single pulse) TLP current needed to create an open structure as a failure criterion, linear scaling behavior is obtained for all structures. This is illustrated in Figure 10. As already discussed before, also the snapback current for silicon based structures scales with width. This is also indicated in Figure 10.

The performance per unit width for metal structures is summarized in Table 1. The ratio between the M3 and M1 performance is equal to the ratio of the metal thickness. The values obtained for the metal structures are in good agreement with the theoretical model in [3], as indicated in Table 1. Per cross section unit area the performance of Al turns out to be 75% of that of Cu. This is related to the lower melt point and larger thermal expansion of Al compared to Cu. The value is close to that found in [6], where it is noted that this ratio also depends on the actual structure (e.g. cladding materials) of the interconnect.

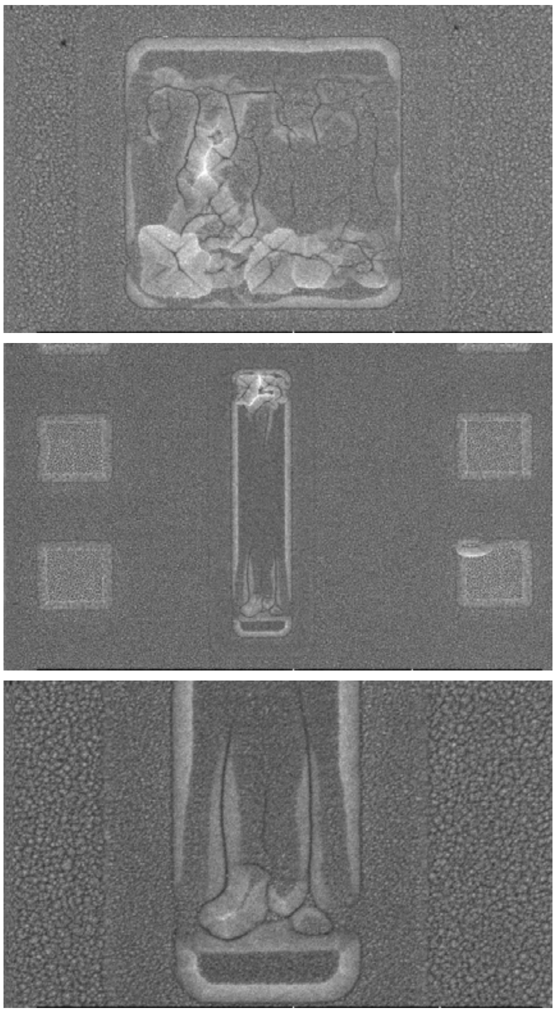

Figure 9: Damages in Si based structures after TLP. Top photo is for unsilicided material, bottom 2 in silicided material.

The performance per unit width for silicon based structures is summarized in Table 2. The fatal current density for these structures is about 5-10 times smaller than that of metal structures in the same technology. Although the fatal current density is quite high, the practical design limitation for ESD robustness is dictated by the snapback current density, which typically is a factor 2-10 lower.

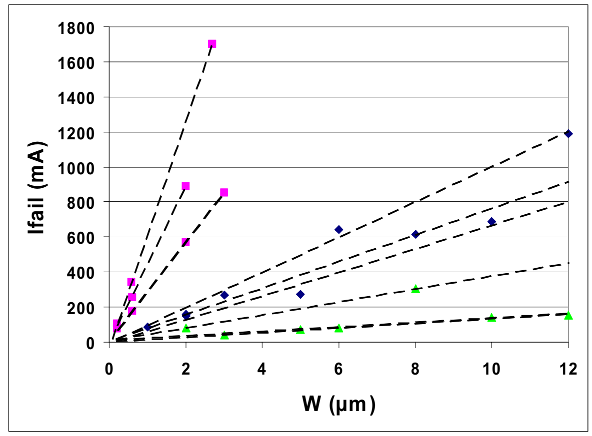

Figure 10: Width scaling for metal based (squares) and silicon based (diamonds and triangles) interconnect. Squares and diamonds indicate open failures, triangles indicate soft failure.

Table 1: Measured (top row) and predicted (bottom row) performance per unit width (mA/µm) for metal interconnect

	Cu, M1	Cu, M3	Al, M6
Jfail, measured (mA/µm)	285	445	640
Jfail, predicted (mA/µm)	350	475	600

Table 2: Performance summary for silicon based interconnect

	Poly	silicide	diffusion
Jsnapback (mA/µm)	13	37	13
Jfail (mA/µm)	100	76	68

D. HBM-TLP Correlation

In order to be able to convert TLP parameters into HBM parameters as typically used by design groups both TLP and HBM tests have been performed on all structures. Failure levels are given together in Figure 11, showing that the correlation is 2 kV HBM per 1 A TLP, which is almost equal to that found theoretically in [3] for interconnect structures and experimentally in [15] on completely different structures. Note that this figure contains data from all types of structures used for this paper. Thus the correlation is shown to be applicable to a wide variety of devices.

E. Repetition

Since it is clear that an ESD pulse can cause a permanent change in the resistance of a metal line it is interesting to see how the resistance develops as a function of multiple stresses. Results of such an experiment are shown in Figure 12. The pulses are given at 95% and 98% of the current that causes an open fail with just 1 pulse (Table 1).

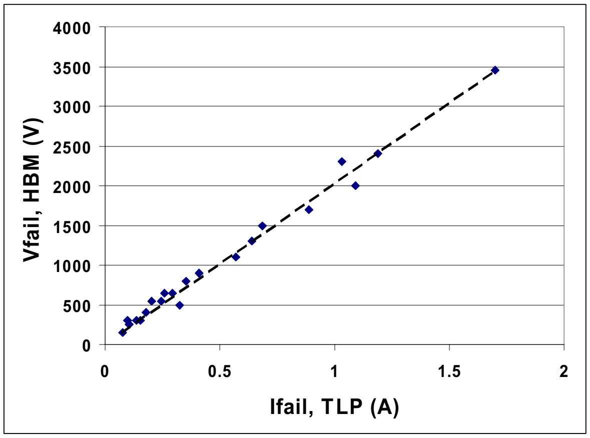

Figure 11: Correlation between HBM and TLP failure level for all structures.

Clearly the number of stresses a sample can sustain, depends strongly on how close the stress is to the critical level. Stresses at 95% do not cause a failure for more than 1000 pulses, but do cause a very small change with every pulse. At 98% the development is quicker, but still more than 100 pulses can be given without causing an open connection. At 99% only a few pulses lead to fatal damage.

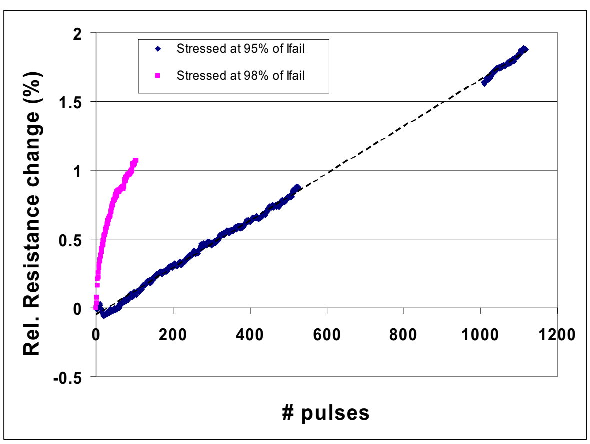

Figure 12: Relative resistance change as a function of number of pulses for different stress currents.

Both samples of Figure 12 were deprocessed to the barrier layer for inspection. The sample that was stressed at 95% did not have any damage visible in a SEM. The other sample showed 2 spots as illustrated in Figure 13. Clearly some lateral and vertical extrusion is visible. Apparently a damage in the barrier layer was just developed.

Thus it is likely that more latent damage can be done by such non-fatal ESD stresses.

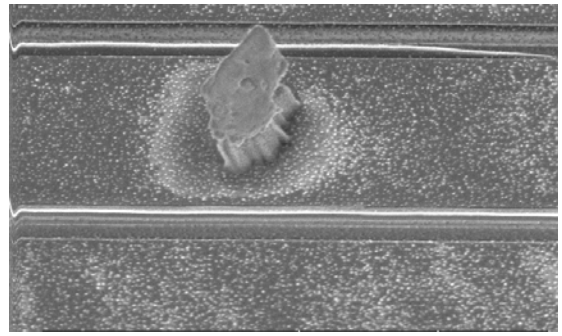

Figure 13: Damage on a line after many low current TLP pulses.

III. Electromigration

As discussed in the previous section ESD stress may lead to subtle resistance changes before fatal damage is observed. It is reported in literature that EM lifetime can be reduced by a factor of 3 by ESD stress [1],[3],[9]. We expect that the EM lifetime is related to the amount of stress that a sample has seen before being subjected to EM testing.

A. EM Results

Therefore, in this study EM tests have been performed both on Al and Cu structures. First the results on the Al samples as used for the ESD study are presented. Samples are ESD pre-stressed at certain percentages of the maximum current (Table 1), with 1 or 10 pulses. As an example the EM time-to-failure data for the 3µm lines are given in Figure 14.

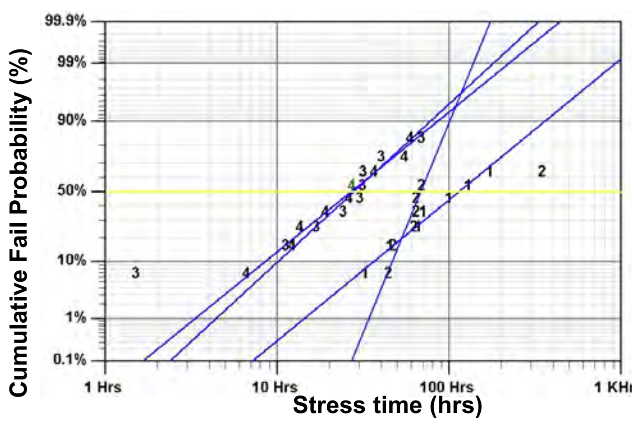

Figure 14: EM Time-To-Failure distribution of 3 µm M6 lines under test conditions. Numbers refer to groups as given in Table 3.

The lifetime under user conditions is obtained by data extrapolation. All results are summarized in Table 2. Clearly ESD stresses in the critical region reduces the EM lifetime dramatically, with impacts seen from both ESD stress level and number of pulses used. In most cases the reduction of the lifetime are much more than the factor of 3 mentioned before, even though the ESD caused resistance change is very small. Note that several groups were stressed at TLP current levels that even after hundreds of pulses only give marginal resistance changes.

Table 3: Extrapolated life time results for ESD pre-stressed Al NIST structures.

W (µm)	Stress level (%)/(Group)	# pulses	Fail Ratio	Life Time (yrs)
3.0	- / (2)	-	7/10	93
3.0	95 / (1)	1	7/10	26
3.0	99 / (3)	1	9/10	9
3.0	98 / (4)	10	9/10	6
0.64	- / (5)	-		>100
0.64	85 / (6)	1	3/10	11
0.64	97 / (7)	1	10/10	26
0.64	95 / (8)	10	2/10	23
0.64	99 / (9)	10	10/10	0.4

In a similar way several Cu NIST structures were ESD pre-stressed and subsequently tested for EM lifetime. For each group 10 samples were used. Lifetime was calculated, with at least 8 samples failed for each split. The effect of the pre-stress on the extrapolated lifetime is illustrated in Figure 15. As for the Al structures a dramatic reduction in lifetime is observed.

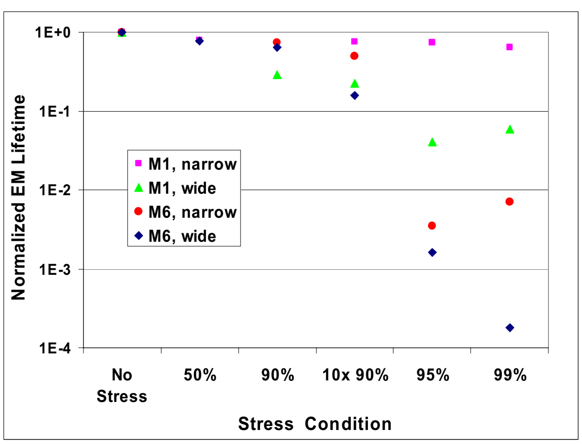

Figure 15: Effect of ESD pre-stress on normalized extrapolated EM lifetime for Cu structures.

B. Failure mode

Damage modes are also studied after EM tests. Normally after DC EM stress a single failure location (open connection) is found, near the cathode side of the structure. For pre-stressed samples often damages at multiple locations are observed, which are randomly distributed over the length of the structure, as shown in Figure 16. This is related to the global rise of the temperature along the length of the line, as reported in [13] for pulses of the TLP time scale.

It is known that due to the high temperatures during TLP melting and recrystallization occurs [7], which leads to smaller grain sizes. In addition the material expands and contracts, leaving some extrusions in the dielectric. This will lead to small micro voids between grains, which form the starting points for EM damage. As shown in Figure 13 even relatively low TLP stress may damage the barrier layer. This will lead to reduced EM lifetime.

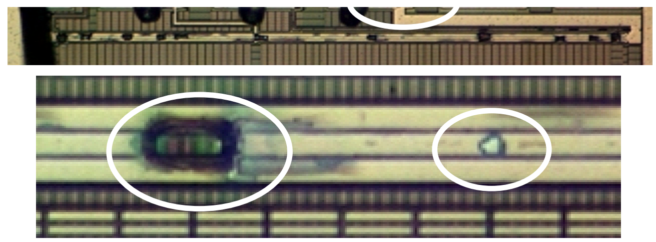

Figure 16: Optical photographs of damaged Al NIST structure: overview and detail with open (left) and discolorization (right).

Several samples were deprocessed down to the metal level by plasma etching. SEM pictures of those are shown in Figure 17. Note that different type of damages are visible, sometimes occurring in the same sample. Also note that the nature is very different from the damage after TLP only (Figure 3 and Figure 13). In all SEM pictures some extrusions are visible.

IV. Conclusions

This paper studied ESD phenomena in interconnect structures. It has been shown that the ESD robustness of both metal based and silicon based interconnect scales linearly with line width. The fatal mechanism is heat driven. Before the fatal damage other mechanisms will occur.

In metal based interconnect this is evident from small permanent resistance changes, that will not lead to functional problems. However the electromigration lifetime can reduce with a factor more than 100.

In silicon based interconnect structures a snapback phenomenon has been observed. This is accompanied by a significant, permanent change in the resistance.

The data obtained enables designers to determine line widths such that during any ESD event, the current density stays well below the critical current density for the given material, taking into account potential reliability issues.

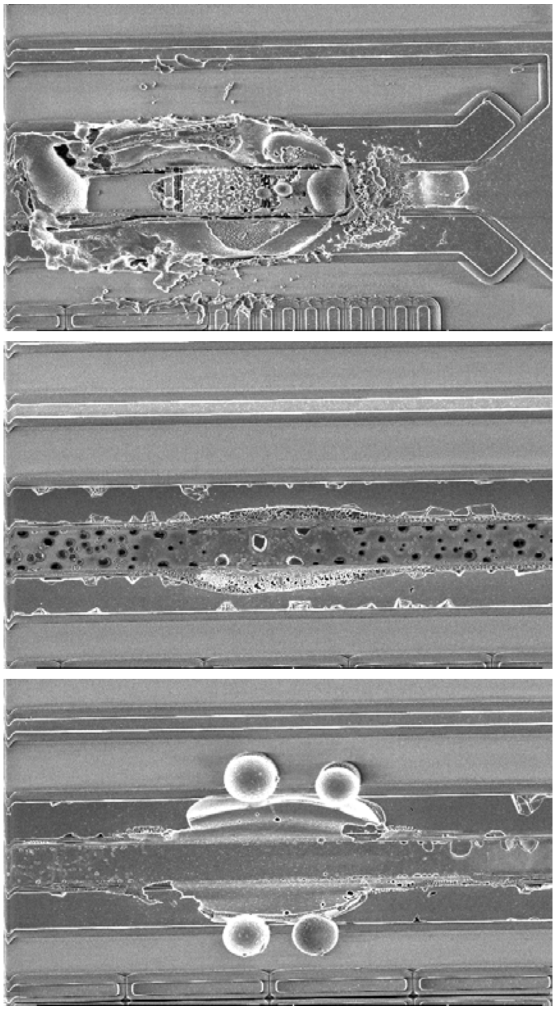

Figure 17: Different damages on Al line after pre-stressed EM.

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